As shown in FIG. 2B, dummy leads 232 are bonded to corner-situated lead-bonding areas 222, thereby providing firm support to the corners of the semiconductor chip and reinforcing the mounting of the semiconductor chip 210 on the tape carrier 220 (see specification at page 6, lines 11-16).

The above-described semiconductor package structure can yield significant benefits. By providing the bonding arrangement of the dummy leads as described above, firm support is provided to the semiconductor chip, and the semiconductor chip is held in position with respect to the tape carrier. Moreover, the mechanical strength of the tape carrier package structure is enhanced (see page 7, lines 5-10).

Claims 1, 5, and 6 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,268,644 to Umehara et al. (hereinafter "Umehara"). Claims 2-4 and 7-12 were rejected under 35 USC 103(a) as being unpatentable over Umehara. For convenience, these rejections are addressed together and are hereby traversed.

Umehara fails to teach or suggest a group of dummy leads which are bonded between dummy pads on the semiconductor chip and corner-situated lead-bonding areas on the tape carrier to provide firm support to the corners of the semiconductor chip, so as to hold the semiconductor chip in position with respect to the tape carrier and to enhance mechanical strength of the tape carrier package structure.

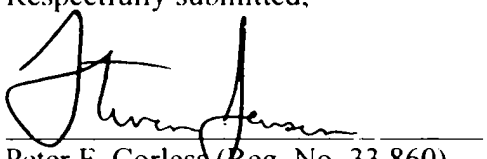
In Umehara, dummy wires 17 are provided as "dam members" to suppress the flow velocity of molding resin in order to prevent adjacent wires from short circuiting (see column 2, lines 40-44). However, the dummy wires 17 do not provide support to the corners of the semiconductor chip. As shown in FIG. 3, when subjected to the flow of molding resin, the wires 17 receive force from the flow and are bent under the influence thereof (see column 4, lines 51-65).

In contrast, the Applicants' claimed invention teaches a group of dummy leads (e.g., as shown in FIG. 2B of the application) which provide support to the semiconductor chip and will not bend like the wires 17 in Umehara. Therefore, the leads as taught in the Applicants' claimed invention are capable of providing support to the semiconductor chip, and thus are structurally different from the dummy wires taught in Umehara. Accordingly, Umehara fails to teach or suggest dummy leads that provide support to the semiconductor chip as recited in the Applicants' claimed invention.

On page 3 of the Office Action, it was noted that the claims did not recite certain features which were included in the arguments accompanying the Amendment of February 12, 2002. Claims 1, 6, and 10 have been amended to more clearly recite important aspects of the Applicants' invention, such that the claims now require a group of dummy leads which are bonded between dummy pads on the semiconductor chip and corner-situated lead-bonding areas on the tape carrier to provide firm support to the corners of the semiconductor chip, so as to hold the semiconductor chip in position with respect to the tape carrier and to enhance mechanical strength of the tape carrier package structure. Umehara neither teaches nor suggests such a structure for the reasons discussed above.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1, 6, and 10 have been amended as follows:

1. (Amended) A tape carrier package structure, which comprises:

(a) a semiconductor chip having:

(a1) a plurality of I/O pads arranged along the sides thereof; and

(a2) a plurality of dummy pads arranged on the corners thereof;

(b) a tape carrier having a device hole for accommodating the semiconductor chip therein and a plurality of side-situated lead-bonding areas and corner-situated lead-bonding areas surrounding the device hole;

(c) a set of inner leads, including:

(c1) a group of I/O leads, which are bonded between the respective I/O pads on the semiconductor chip and the side-situated lead-bonding areas on the tape carrier, so as to allow the semiconductor chip to be electrically connected to the tape carrier by the I/O leads; and

(c2) a group of dummy leads, which are bonded between the respective dummy pads on the semiconductor chip and the corner-situated lead-bonding areas on the tape carrier, and thereby provide firm support to the corners of the semiconductor chip, so as to hold the semiconductor chip in position with respect to the tape carrier and to enhance mechanical strength of the tape carrier package structure.

6. (Amended) [An] A tape carrier package structure, which comprises:

(a) a semiconductor chip having:

(a1) a plurality of I/O pads arranged along the sides thereof; and

(a2) a plurality of dummy pads arranged on the corners thereof;

(b) a tape carrier having a device hole for accommodating the semiconductor chip therein and a plurality of side-situated lead-bonding areas and corner-situated lead-bonding areas surrounding the device hole;

(c) a set of inner leads, including:

(c1) a group of I/O leads, which are bonded between the respective I/O pads on the semiconductor chip and the side-situated lead-bonding areas on the tape carrier, so as to allow the semiconductor chip to be electrically connected to the tape carrier by the I/O leads; and

(c2) a group of dummy leads, which are bonded between the respective dummy pads on the semiconductor chip and the corner-situated lead-bonding areas on the tape carrier, and thereby provide firm support to the corners of the semiconductor chip, so as to hold the semiconductor chip in position with respect to the tape carrier and to enhance mechanical strength of the tape carrier package structure, and which are spaced at substantially the same pitch as the I/O leads.

10. (Amended) A tape carrier package structure, which comprises:

(a) a semiconductor chip having:

(a1) a plurality of I/O pads arranged along the sides thereof; and

(a2) a plurality of dummy pads arranged on the corners thereof;

(b) a TAB tape having a device hole for accommodating the semiconductor chip therein and a plurality of side-situated lead-bonding areas and corner-situated lead-bonding areas surrounding the device hole;

(c) a set of inner leads, including:

(c1) a group of I/O leads, which are bonded between the respective I/O pads on the semiconductor chip and the side-situated lead-bonding areas on the TAB tape, so as to allow the semiconductor chip to be electrically connected to the TAB tape by the I/O leads; and

(c2) a group of dummy leads, which are bonded between the respective dummy pads on the semiconductor chip and the corner-situated lead-bonding areas on the TAB tape, and thereby provide firm support to the corners of the semiconductor chip so as to hold the semiconductor chip in position with respect to the tape carrier and to enhance mechanical strength of the tape carrier package structure, and which are spaced at substantially the same pitch as the I/O leads.